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Inventor

: Zhang Fan

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#### Remarks/Arguments

Examiner Picardat is thanked for the thorough Office Action.

#### In the Claims

Claims 17 to 27 (Group 1) are canceled as per the restriction requirement.

Claim 28 is amended. For support see figure 1. See spec p 9 to p. 17. The conductive buffer layer is conductive (Spec P. 12 L 11). The bond pad support layer 42 is conductive (see Spec. p. 14, LL 17-20). The bond pad is conductive. See spec. p. 15, L 20). It is known to those skilled in the art that bond pads are electrically connected to the underlying connected wiring layers as shown in figure 1.

New dependent claims 29 to 32 (from parent claim 28) are added. For supports see claims 2 to 15.

New parent claim 33 is added. For support see claims 1 and amended claim 28. Claim 31 does not claim the "bond pad support" (as claimed in amended claim 28).

> Dependent claims 34 to 38 are added. For support see claims 1 to 15. No new matter is added.

#### **ELECTION/RESTRICTIONS**

Applicant elected with traverse Group II claims 1-3, 5-15, & 28 in the previous response.

Applicant acknowledges the final requirement of the traverse of the invention non-elected Group I - claims 17 to 27.

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Please cancel non-elected claims 17 to 27. These claims will be prosecuted in a divisional patent application at a later date.

# Rejection of Claim 28 is under 35 U.S.C.102(e) as being anticipated by Balakumar et al. US 6,830,971.

The rejection of Claim 28 is under 35 U.S.C.102(e) as being anticipated by Balakumar et al. US 6,830,971. is acknowledged. Reconsideration and withdrawal is respectfully requested in view of the amendments to the claims and following remarks.

#### The instant office action states:

Balakumar et al. teaches a method of forming a bond pad structure including providing a top wiring layer and a top dielectric (200) over a 'substrate, forming a dielectric layer (21) over the top wiring end dielectric layer, forming an opening in the dielectric layer, forming a pad (25) in the opening, forming a passivation layer (22) over the pad and dielectric, forming an opening in the passivation layer, and forming a bond pad (290) and bond pat support in the opening (see figs 2A-2C and related text).

Amended claim 28 is non-obvious over the 6,830,971

Table A below compares Amended clam 28 with US 6,830,971.

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Table A -	
Applicant's Claim 28	US 6,830,971
28. (currently amended) A method of fabrication of a	Different - Method to form a Capacitor, not a bond
bond pad structure, comprising the steps of:	pad. See abstract, see all claims.
providing a top wiring layer and a top dielectric	Different - Figure 2A - Does not show the top wiring
layer over a semiconductor structure;	layer, only shows a middle wiring layer 25.
forming a buffer dielectric layer over said top wiring	different – non-analogous elements
layer and said top dielectric layer;	
forming a buffer opening in said buffer dielectric	different- non-analogous elements
layer exposing at least of portion of said top wiring	
layer;	
forming a buffer pad in said buffer opening;	different- non-analogous elements
forming a passivation layer over said buffer pad and	different -non-analogous elements
said buffer dielectric layer;	·
forming a bond pad opening in said passivation layer	different non-analogous elements
over at least a portion of said buffer pad;	
forming a bond pad and bond pad support at least in said bond pad opening;	Different - does not suggest the bond pad support
said bond pad is electrically connected to said buffer pad.	Different – The capacitor dielectric layer 27 electrically insulated the first metal electrode 25 and the second metal electrode 290. See figure 2C. See col 7, line 13-15.

US 6,830,971 does not suggest claim 28's bond pad structure

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First, US 6, 830,971 discloses a capacitor having a capacitor dielectric layer between two capacitor electrodes. The capacitor dielectric layer is an insulator designed to not allow conduction between the first and second electrodes. See table above (last step).

Also, the plain meaning of "top wiring layer" is the upper most wiring layer.

The terms "top wiring layer" and upper most wiring layer known to those skilled in the art.

The spec. p. 10 Lines 9- 13 states:

The top wiring layer is the upper most interconnecting layer (e.g., metal level 6 in a 6 metal layer IC). Typically, under the top metal layer 22 and top dielectric layer are levels of wiring and inter metal dielectric layers.

In contrast, US 6,830,971 shows a capacitor on a *middle* (not top) level wiring layer.

#### Showings under 37 CFR 1.132 or 37 CFR 1.131.

The office action further states:

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

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Applicant thanks the examiner for providing these options. Applicant feels that the present claims are non-obvious over the cited patent. However, applicant may pursue one of these options in the future.

# New dependent claims 29 to 32 are non-obvious

New dependent claims 29 to 32 (from parent claim 28) are non-obvious because they depend from non-obvious parent claim 28 for the reasons stated above. Claim 29 to 32 also contain further non-obvious limitations.

## New Parent claim 33

# New parent claim 33 states:

33 (NEW) A method of fabrication of a bond pad structure, comprising the steps of: providing a top wiring layer and a top dielectric layer over a semiconductor structure; forming a buffer dielectric layer over said top wiring layer and said top dielectric layer; forming a buffer opening in said buffer dielectric layer exposing at least of portion of said top wiring layer;

forming a buffer pad in said buffer opening;

forming a passivation layer over said buffer pad and said buffer dielectric layer;

forming a bond pad opening in said passivation layer over at least a portion of said buffer

forming a bond pad at least in said bond pad opening; said bond pad is electrically connected to said buffer pad.

Claim 33 is non-obvious for the reasons discussed above for claim 28 less the element of the "bond pad support".

## Dependent claims 34 to 38 are non-obvious

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New dependent claims 34 to 38 are non-obvious because they depend from non-obvious parent claim 33 for the reasons stated above. Claims 34 to 38 also contain further

non-obvious limitations.

ALLOWABLE SUBJECT MATTER

The allowance of claims 1-3 and 5-15 is gratefully acknowledged.

**CONCLUSION** 

In conclusion, reconsideration and withdrawal of the rejections are respectfully requested. Allowance of all claims is requested. Issuance of the application is requested.

It is requested that the Examiner telephone the undersigned attorney at (215) 670-2455 should there be anyway that we could help to place this Application in condition for Allowance.

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# **Charge to Deposit Account**

The Commissioner is hereby authorized to apply any fees or credits in this case, which are not already covered by check or credit card, to Deposit Account No. 502018 referencing this attorney docket. The Commissioner is also authorized to charge any additional fee under 37 CFR §1.16 and 1.17 to this Deposit Account.

Respectfully submitted,

Date: 7/13/05

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Computer file info: us02-101-roa2-dated-2005-06-16.doc

file size: 86528

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PTO/SB/08 (12-04)
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(37 CFR 1.18()) N/A OR N/A 50.00 TOTAL TOTAL \$0.00 OR ADD'L. FEE ADD'L FEE (Column 1) (Column 2) (Column 3) HIGHEST NUMBER PREVIOUS ADDI CLAIMS REMAINING ADDI-TIONAL PRESENT TIQNAL RATE (5) Œ RATE (\$) **EXTRA** AFTER AMENDMENT FEE (\$) FEE (\$) PAID FOR AMENDMENT Total (37 CFR 1.16(i)) OR 00.02 50 26 Minus 0 2 OR ¥ \$0.00 Independent (37 CFR 1.16(h)) 200 0 Minus 00.02 Application Size Fee (37 CFR 1.18(6)) FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.18(I)) NA OR N/A 00.02 TOTAL TOTAL OR \$0.00 ADD'L FEE ADD'L. FEE " if the entry in column 1 is less than the entry in column 2, write "0" in column 3.

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This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.